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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,215	07/09/2003	Uwe Meding	CHIP 2720000	1728

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,215	MEDING, UWE	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/616,215 filed 07/09/2003.

2. Claims 1-7 are pending in the Application.

Drawings

3. The drawings are objected to because Figures 8 and 9 do not have arrows between components like it shown in the Figure 7. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 1-6 are objected to because of the following informalities:

in the claims 1 and 2 in the limitations (a) and (b) Applicant must distinguish vertices in the first and second lists by labeling them differently, for example, "first unique vertex" - for the limitation (a) and "second unique vertex" – for the limitation (b);

claim 1 in the limitation (g) has an insufficient antecedent basis issue, as there is no indication of storing list in the previous limitations of the claim;

claim 3 in the limitation (g) has an insufficient antecedent basis issue as there is no indication of storing the discrepancy list in the previous limitations;

claim 4 limitation (b) "deleting . . ." from where?

claim 5 limitation (e) "computer code for removing any vertexes . . ." from where?

claim 6 limitations (c), (f), (h) ". . . for deleting any vertexes . . ." from where?

claim 7 limitations (c), (f), (h) removing vertexes from where?

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is: a condition during comparison of

two lists on which removal of matching vertices is based, for example "if the first unique vertex in the first list matches with the second vertex in the second list, then . . . "

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Barke et al. ("A Network Comparison Algorithm for Layout Verification of Integrated Circuits" April 1984, IEEE Transactions on, Volume 3, Issue 2, Page(s):135–141).

With respect to claims 1, 5 Barke et al. teaches a method of electronically comparing two circuits for identicalness within verification method for testing two circuits by comparison algorithm to test isomorphism (page 135, left column), a computer program product fir ascertaining the identicalness of two circuits, the computer program product having a medium with a computer program embodied thereon within implementation the computer program NECOM for performing comparison of two integrated circuits represented by graphs using isomorphism test (page 135, left column), wherein NECOM program is written in the language Pascal (abstract; page 140, left column), comprising: (a) compiling, within one or more-memories, a first list of all components in a first circuit, said first list including data relative to all connections of each component listed, each component in said first list hereinafter being referred to as a vertex within a disk file containing the components and interconnections of the actual

(first) circuit (page 135, right column), wherein first (actual) circuit is represented as a graph G^1_p having nodes (vertices) as shown on the Fig. 2(b) for further circuit analysis (abstract; page 137, left column); (b) compiling, within one or more memories, a second list of all components in a second circuit, said second list including data relative all connections of each component listed, each component in said second list hereinafter being referred to as a vertex within a nominal circuit obtained from the design system (page 135, right column) whish is used for comparison with the actual circuit (page 135, left column) and represented as graph G_p as shown on the Fig. 2(a) (page 137, left column); (c) comparing, within one or more processors, each unique vertex in said first list with unique vertexes in said second list within mapping G_p onto G^1_p (page 137, left column); (d) removing matching vertexes from said first and second lists within identifying matched unique nodes (vertices) p/p^1 in the graphs G^1_p and G_p and removing them from the lists (page 138, left column); (e) generating, within one or more processors, a discrepancy listing of unmatched unique vertexes in said first and second lists by reporting the differences if the circuits are not identical during the comparison (page 136, right column) and within generating a report conflict as shown in Dif. 3 (page 136, right column); (f) removing the unique vertexes from said first and second lists that were placed in the discrepancy listing within removing matched nodes (vertices) from the node lists to reduce list processing time (page 138, left column); (g) compiling, within one or more memories, new first and second lists of all remaining vertexes of previous first and second lists expanded in scope by one vertex attached to each connection of the previous list stored by initiating a new matching cycle with remaining

nodes (page 138, left column); (h) comparing, within one or more processors, each unique vertex in said new first list with unique vertexes in the new second list within the gradual progress in matching nodes and spiders as shown in the flow diagrams in the Figures 4 and 5 within the matching process in the iterative mode as shown in the Fig. 3 (page 138, right column); (i) removing matching vertexes from said first and second lists within removing matched nodes (vertices) from the node lists to reduce list processing time (page 138, left column); (j) adding to said discrepancy listing any remaining unmatched unique vertexes in said new first and second lists within finding an additional device between actual circuit and nominal circuit and gradually progress in matching nodes and spiders (page 138, right column); (k) removing the unique vertexes from said new first and second lists that were added to the discrepancy listing in step (j) within removing matched nodes (vertices) from the node lists to reduce list processing time (page 138, left column); and (l) repeating steps (g) through (k) until all vertexes have been uniquely defined within calling the operation "MATCH" of the program NECOM again, wherein the comparison algorithm for test isomorphism (page 135, left column) begins again to loop until no further spiders (vertices) or nodes (vertices) can be matched (page 139, right column).

With respect to claim 2 Barke et al. teaches the same subject matter as was claimed in the claim 1, additionally disclosing that the isomorphism test can be executed by N! comparison operations (page 136, left column), wherein partitioning of the nodes in the graph into several groups is involved (page 136, left column) and some partitions contain only one element, while comparison operation is extended by second phase of

the comparison algorithm, wherein the neighborhood (additional component connected to each connection of prime component) of each matched device or net is considered (page 136, right column).

With respect to claims 3, 4, 6 and 7 Barke et al. teaches the same subject matter as was claimed in the claims 1 and 2, additionally disclosing that the isomorphism test can be executed by N! comparison operations (page 136, left column); including implementation of the program NECOM, using available main memory (page 140, right column) and creating first and second lists of signatures for all vertices in first and second circuits respectively, the signatures having a given minimal scope and stored in one or more memories by partitioning of the nodes in the graph into several groups having the small number of nodes in the partitions (minimal scope) (page 136, left column), wherein some partitions contain only one element (page 136, right column), , while comparison operation is extended by second phase of the comparison algorithm, wherein the neighborhood (signatures) of each matched device or net is considered (page 136, right column), including implementation the computer program NECOM for performing comparison of two integrated circuits represented by graphs using isomorphism test (page 135, left column), wherein NECOM program is written in the language Pascal (abstract; page 140, left column).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
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